Gabriel Feng

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Research Interest

Pursuing graduate study in semiconductor devices with a focus on fundamental research in device physics, fabrication, and characterization. I bring experience from both industry settings, such as semiconductor metrology at Samsung, and research cleanroom environments developing and characterizing advanced electronic and photonic devices.

Education

Georgia Institute of Technology *Expected May 2026*

B.S. in Physics & B.S. in Electrical Engineering; AI/ML minor

- **GPA:** 3.97/4.0
- **Societies:** College of Science Dean's Scholar, President's Undergraduate Research Award, SCALE DoD HIAP Scholar
- **Relevant Coursework:** Semiconductor Devices, IC Fabrication, Advanced Packaging, Analog IC Design, Solid State Physics, Quantum Mechanics, Quantum Information and Computing, Statistical Mechanics, Machine Learning

Skills

Semiconductor Equipment: 1000+ hours ISO 5 Cleanroom experience; Deposition (ALD, PEALD, CVD, PECVD, PVD), Oxidation/doping furnace, Photoresist Spinner, Masked/Maskless Aligner, RIE, Wet Etch, E-beam/UV Lithography, Dicer

Characterization: Reflectometer, Profilometer, Resistance Probe, SEM, AFM, Raman, Ellipsometer, Oscilloscope, Dark-field

Vendors: Applied Materials, TEL, Plasma-Therm, Canon, Cambridge, Oxford, Tystar, Karl Suss, KLA Tencor, Horiba

Software: Python, Java, VHDL, MATLAB, Spotfire, SPC, JMP, SQL, CAD, TCAD, tensorflow, COMSOL, Linux, LaTeX

Fabrication: CNTFEA, FISCT-T, MOSFET, Ring Osc., Capacitors, Resistors, FinFET (Metrology), SLCFET (ALD/PECVD)

Research

GTRI – Center for Space Hardware Assembly, Fabrication and Testing *Atlanta, GA*

Research Intern *May 2023 – Present*

- Researched Carbon Nanotube Field Emission Arrays (CNTFEAs) for Hall Effect thruster applications
- Directed a 28-step semiconductor process integration flow for CNTFEA chips in Georgia Tech's IEN cleanroom facilities
- Iteratively refined process parameters including etch chemistry, deposition time, doping conditions, and metrology recipes
- Validated CNT field emission using a custom LabView-controlled high-voltage system, confirming tunneling behavior
- Awarded President's Undergraduate Research Award to investigate alternative gate thin films for triode-type CNTFEAs
- Performed structural and electrical characterization of sub-10 µm features using SEM, reflectometry, profilometry, and spectroscopy, diagnosing and troubleshooting fabrication deviations
- Generated detailed process documentation and specifications for CNTFEA fabrication, enabling reproducibility/scaling
- Presented a poster at the TMS 2025 Annual Meeting, showcasing CNTFEA fabrication and device optimization results

Integrated 3D System Packaging *Atlanta, GA*

Undergraduate Researcher *Oct 2024 – Present*

- Fabricated micro-packages using TSHs and angled surface-coupling waveguide designs for optical fiber integration
- Patterned, developed, and cured positive self-alignment structure (PSAS) for sub-micron alignment
- Demonstrated low <2 dB insertion loss in passive test structures through precision process development
- Performed testing and optical probing to validate alignment, coupling efficiency, and structural integrity

Epigraphene Lab *Atlanta, GA*

Undergraduate Researcher *Apr 2023 – Dec 2024*

- Fabricated epitaxial graphene sample chips using standard cleaning, resist spinning, and custom vacuum furnace baking
- Revived ellipsometer and created recipes for accurate characterization of BN layers (2–20 nm); verified with AFM
- Performed NMF-based deconvolution for Raman spectra analysis of graphene G and 2D peaks
- Designed, assembled, and calibrated low-temperature PVD furnace for selenium with HV chamber components
- Built a vacuum four-point van der pauw probe station to measure graphene samples under controlled conditions

Experience

Samsung Semiconductor *Austin, TX*
Metrology Applications Intern *May 2025 – Aug 2025*

- Identified and analyzed critical defects in 14 nm FinFET technology using dark-field inspection and SEM review
- Developed a cloud-based scoring application to proactively evaluate darkfield scan recipes and enhance pre-VOC readiness
- Integrated a CNN based signature detection algorithm to validate scan accuracy and flag recipe/device weaknesses
- Conducted optics selector studies across dielectric and metal films, achieving up to 117% defect detection improvement
- Documented polarization for film/topography-dependent laser scattering for process-level tuning for 4 nm node fab
- Investigated and characterized defects of interest, collaborating with process and yield teams to perform FMEA

Northrop Grumman Advanced Technology Lab *Linthicum, MD*
Semiconductor Process Engineering Intern *May 2024 – Aug 2024*

- Maintained (PE)ALD and (PE)CVD films for pHEMT, SLCFET, HBT devices and ensured process specs using SPC
- Performed a study on stress of ALD-grown films and determined the plasma/thermal Al_2O_3 ratio for net zero stress films
- Reduced contact angle on PECVD Si_3N_4 films by ∼80%, optimizing surface energy for photoresist primer
- Created in-situ plasma surface termination recipe for contact angle tuning between 5°–60° without degrading film quality
- Developed Python script to predict precursor cycle limits prior to ALD tool fault, recovering wafer lot in production

High-Altitude Balloon Research *Atlanta, GA*
Electronics Lead *Aug 2022 – May 2023*

- Led design and construction of experimental apparatus for integration with Georgia Tech's Low Turbulence Wind Tunnel
- Coordinated with multidisciplinary team members to determine logistics and implement parachute deployment and payload design
- Fabricated load cell interface and programmed system (C++ and Bash) to measure drag force across parachute reefing states
- Designed and programmed reefing crank to optimize descent rate, achieving a 30% reduction in descent time

Teaching Assistant *Atlanta, GA*
Georgia Tech PHYS 2211 *January 2023 – May 2023*

- Facilitated weekly lab sessions by setting up and maintaining experimental equipment
- Led discussion sections focused on mechanics concepts, guiding students through problem-solving strategies
- Provided one-on-one academic support during office hours, reinforcing lecture material
- Graded lab reports, homework, and exams with attention to accuracy and fairness

Tutoring Academic Support (TAS) *Atlanta, GA*
Academic Tutor *January 2023 – 2024*

- Tutored undergraduate students across a range of subjects, from introductory mathematics through quantum mechanics
- Conducted one-on-one and small-group sessions, adapting explanations to diverse learning styles
- Reinforced problem-solving skills and conceptual understanding to strengthen student performance in STEM courses

Publications & Conferences

- S. Yu, G. Feng, T. K. Gaylord, and M. S. Bakir, "Self-Aligned Fiber Coupling using Tilted-Si Chiplets for Photonic Integration," *IEEE Photonics Technology Letters vol. 37, 2025*, (under revision).
- G. Feng, et al., "Alternative Gate Thin Films for Triode-Type CNTFEAs," Poster presented at *TMS Annual Meeting & Exhibition*, Las Vegas, NV, March 2025.

References

Dr. Jud Ready – Executive Director of the Space Research Institute, Georgia Tech Research Institute
Dr. Muhannad Bakir – Director, 3D Systems Packaging Research Center, Georgia Institute of Technology
Dr. Thomas Gaylord – Regents' Professor, Georgia Institute of Technology
Dr. Chaoyue Becker – Metrology Applications Manager, Samsung Semiconductor
Dr. Junsic Hong - CVD Manager, Northrop Grumman Advanced Technology Lab