

Gabriel Feng

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Education

Massachusetts Institute of Technology

Aug 2026 – Present

Ph.D. in Electrical Engineering and Computer Science (EECS)

- Analog Devices Stata Family Presidential Fellow

Georgia Institute of Technology

May 2026

B.S. in Physics & B.S. in Electrical Engineering; AI/ML minor

- **GPA:** 3.97/4.0
- **Honors:** College of Science Dean's Scholar, President's Undergraduate Research Award, SCALE DoD HIAP Scholar
- **Relevant Coursework:** Semiconductor Devices, IC Fabrication, Advanced Packaging, Analog IC Design, Solid State Physics, Quantum Mechanics, Quantum Information and Computing, Statistical Mechanics, Machine Learning

Skills

Semiconductor Equipment: 500+ hours ISO 5 Cleanroom experience; Deposition (ALD, PEALD, CVD, PECVD, PVD), Oxidation/doping furnace, Photoresist Spinner, Masked/Maskless Aligner, RIE, Wet Etch, E-beam/UV Lithography, Dicer

Characterization: Reflectometer, Profilometer, Probing, SEM, AFM, Raman, Ellipsometer, Oscilloscope, Darkfield

Vendors: Applied Materials, TEL, Plasma-Therm, Canon, Cambridge, Oxford, Tystar, Karl Suss, KLA-Tencor, Horiba

Software: Python, Java, VHDL, MATLAB, Spotfire, SPC, JMP, SQL, CAD, TCAD, TensorFlow, COMSOL, Linux, $\text{\LaTeX}$

Fabrication: CNTFEA, FISCT-T, MOSFET, Ring Osc., Capacitors, Resistors, FinFET (Metrology), SLCFET (ALD/PECVD)

Research

MIT – Advanced Semiconductor Devices Lab

Cambridge, MA

Graduate Researcher | PI: Prof. Tomás Palacios

Aug 2026 – Present

- Developing GaN HEMTs with 100 nm L_{SD} and graded $\text{Al}_x\text{Ga}_{1-x}\text{N}$ devices for high-voltage operation
- Characterizing graded AlGa_N etch rates; 2D device modeling in TCAD and exploring ML-enhanced quantum transport
- Calibrating 2D device fabrication with e-beam lithography dose tests and probing transfer length method (TLM) contacts

GTRI – Center for Space Hardware Assembly, Fabrication and Testing

Atlanta, GA

Research Intern | PI: Prof. Jud Ready

May 2023 – May 2026

- Integrated a 28-step process flow for carbon nanotube field emission array (CNTFEA) chips for Hall effect thrusters
- Iteratively refined process parameters including etch chemistry, deposition time, doping conditions, and metrology recipes
- Validated CNT field emission using a custom LabVIEW-controlled high-voltage system, confirming tunneling behavior
- Awarded President's Undergraduate Research Award to investigate alternative gate thin films for triode-type CNTFEAs
- Characterized sub-10 μm features using SEM, EDS, reflectometry, and profilometry to diagnose fabrication deviations

Integrated 3D System Packaging

Atlanta, GA

Undergraduate Researcher | PIs: Prof. Muhannad Bakir, Prof. Thomas Gaylord

Oct 2024 – May 2026

- Fabricated micro-packages using TSHs and angled surface-coupling waveguide designs for optical fiber integration
- Patterned, developed, and cured positive self-alignment structures (PSAS) for sub-micron alignment accuracy
- Demonstrated optical coupling with <2 dB loss in passive grating coupler waveguides through tilted chiplet assembly

Epigraphene Lab

Atlanta, GA

Undergraduate Researcher | PIs: Prof. Claire Berger, Prof. Walter de Heer

Apr 2023 – Dec 2024

- Revived ellipsometer and created recipes for accurate characterization of BN layers (2–20 nm); verified with AFM
- Performed NMF-based deconvolution for Raman spectra analysis of graphene G and 2D peaks
- Designed, assembled, and calibrated low-temperature PVD furnace for selenium with HV chamber components
- Built a vacuum four-point Van der Pauw probe station to measure graphene samples under controlled conditions
- Characterized carrier density and mobility of graphene samples through Hall effect and Van der Pauw measurements

Experience

IBM Research

Albany, NY

Semiconductor R&D Intern | Supervisor: Dr. Will Green

May 2026 – Aug 2026

- Designed co-packaged optics (CPO) devices; collaborated on process integration with IBM Research Zurich and Bromont
- Designed an adiabatic mono-taper for a 44% footprint reduction in IBM CPO, taped out in 2027-generation modules
- Developed 3D photonic integration EDA software using A* and negotiated-congestion algorithms with photonic-aware heuristics
- Migrated Sentaurus TCAD (SWB) CFET decks to SPython and built an internal agent to automate the migration

Samsung Semiconductor

Austin, TX

Metrology Applications Intern | Supervisor: Dr. Chaoyue Becker

May 2025 – Aug 2025

- Identified and analyzed critical defects in 14nm FinFET technology using darkfield inspection and SEM review
- Developed a cloud-based scoring application to proactively evaluate darkfield scan recipes and enhance pre-VOC readiness
- Integrated a CNN-based signature detection algorithm to validate scan accuracy and flag recipe/device weaknesses
- Conducted optics selector studies across dielectric and metal films, achieving up to 117% defect detection improvement
- Documented polarization for film/topography-dependent laser scattering for process-level tuning at the 4nm node
- Investigated and characterized defects of interest, collaborating with process and yield teams to perform FMEA

Northrop Grumman Advanced Technology Lab

Linthicum, MD

Semiconductor Process Engineering Intern | Supervisor: Dr. Junsic Hong

May 2024 – Aug 2024

- Maintained (PE)ALD and (PE)CVD films for pHEMT, SLCFET, and HBT devices, ensuring process specs via SPC
- Performed a study on stress of ALD-grown films and determined the plasma/thermal Al₂O₃ ratio for zero-stress films
- Reduced contact angle on PECVD Si₃N₄ films by ~80%, optimizing surface energy for photoresist primer
- Created in-situ plasma surface termination recipe for contact angle tuning between 5°–60° without degrading film quality
- Developed a Python script to predict precursor cycle limits prior to ALD tool fault, recovering a production wafer lot

CMOS Simulation, Fabrication, and Characterization

Atlanta, GA

IC Fabrication (ECE 4452)

Aug 2024 – Dec 2024

- Modeled IC physical parameters such as junction depth and dopant concentration to refine fabrication process flow
- Created and tested CMOS circuits using a basic CMOS manufacturing procedure and analyzed non-ideal behaviors
- Compiled a process design project correlating fabricated IC performance with process-induced non-idealities
- Fabricated PMOS/NMOS, Van der Pauw structures, logic gates, capacitors, and ring oscillators
- Tested final devices and characterized IV curves of 2 μm transistors, oscillator clock cycles, and resistances

High-Altitude Balloon Hardware Integration

Atlanta, GA

Electronics Lead

Aug 2022 – May 2023

- Led design and construction of experimental apparatus for integration with Georgia Tech's Low Turbulence Wind Tunnel
- Fabricated load cell interface and programmed systems to measure drag force across parachute reefing states
- Designed and programmed reefing crank to optimize descent rate, achieving a 30% reduction in descent time

Georgia Tech Physics Teaching Assistant and Drop-in Tutor

Atlanta, GA

Georgia Institute of Technology

Jan 2023 – Dec 2024

- Lectured before labs on core physics concepts and demonstrated equipment/software usage to students
- Graded lab reports and collaborated with professors to optimize delivery of lab material for classes of ~200 students
- Tutored students one-on-one in math and physics (through 3000-level), developing creative problem-solving strategies

Publications & Conferences

- S. Yu, G. Feng, T. K. Gaylord, and M. S. Bakir, "Self-Aligned Fiber Coupling using Tilted-Si Chiplets for Photonic Integration," *IEEE Photonics Technology Letters*, 2026 (under revision).
- G. Feng and J. Ready, "Alternative Gate Thin Films for Triode-Type CNTFEAs," Poster presented at *TMS Annual Meeting & Exhibition*, Las Vegas, NV, March 2025.